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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/753,766	12/29/2000	Udo Walterscheidt	2207/10124	3472

7590 12/04/2003

KENYON & KENYON
Suite 600
333 W. San Carlos Street
San Jose, CA 95110-2711

EXAMINER	
O'BRIEN, BARRY J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 12/04/2003 6

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/753,766	WALTERSCHEIDT ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with th correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2000 and 19 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-19 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Declaration Fee as received on 4/19/2001, Formal Drawings as received on 4/19/2001, and Filing Receipt as received on 2/24/2003.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 15-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Regarding claims 15-19, they all recite a preamble that does not provide the correct antecedent basis for the claim. These claims recite "a method for concealing switch latency in a multi-threading processor", while their cited parent claim recites "a set of instructions residing in

a storage medium, said set of instructions capable of being executed by a processor for searching data stored in a mass storage device." The preamble recited in these claims is the same as that in claims 9-13. The examiner is unsure whether an editorial mistake was made, or whether these claims are to be interpreted differently from their parent claim. For the purposes of this examination, the examiner will assume that the bodies of these claims are correct, and read them in light of the preamble of their recited parent claim. Please correct the claim language in these claims to more clearly recite and point out was the applicant regards as the invention and provide correct antecedent basis for these claims.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-4, 6-9 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627, in further view of Bondi et al., U.S. Patent No. 5,881,277.

9. Regarding claims 1, 8 and 14, taking claim 1 as exemplary, Parady has taught a multi-threading processor, comprising:

a. A front-end module (14 of Fig.3),

b. An execution module (41 of Fig.3) coupled to said front end module,

c. A state module coupled to said front-end module and said execution module (see 48, 50, 110 of Fig.3). While not shown explicitly as a module, the state module's

function, as described in the Applicant's specification, is encompassed by 48, 50, and 110 of Fig.3, which further shows the required interconnections,

d. A switch logic module (112 of Fig.3) coupled to said state module, wherein said switch logic module detects a long-latency event in a software thread and schedules a switch to another software thread during a latency of said long-latency event (see Col.3 lines 57-65).

10. Parady has not taught that the switch logic detects a mispredicted branch in a thread and schedules a switch to another thread during the latency of the mispredicted branch.

11. However, Bondi has taught that a branch misprediction event will result in large performance penalties, costing many cycles in order to fetch the correct path's instructions (see Col.1 lines 47-64). One of ordinary skill in the art would have recognized that increasing processor performance and throughput are of paramount concern to designers. Therefore, one of ordinary skill in the art would have found it obvious to modify Parady to also detect mispredicted branch events and schedule a switch to another software thread, in a manner similar to how Parady handles load instructions, in order to reduce the performance penalty suffered by the misprediction.

12. Claims 8 and 14 are nearly identical to claim 1. They differ in their lack of explicit hardware modules, but are both methods that encompass the same scope as claim 1. Therefore, claims 8 and 14 are rejected for the same reasons as claim 1.

13. Regarding claim 2, Parady in view of Bondi has taught a multi-threading processor as recited in claim 1, wherein the switch logic module detects a switching event (see Parady, Col.3 lines 57-65).

14. Regarding claim 3, Parady in view of Bondi has taught a multi-threading processor as recited in claim 2, wherein the switch logic module includes a cache miss indicator that is set when a cache miss is detected and reset when the switch is completed (see Parady, 114 of Fig.3 and Col.3 lines 57-64), but has not explicitly taught a mispredicted indicator that is set when a branch is mispredicted.

15. However, Bondi has taught a mispredicted signal (see Fig.2, and Col.6 lines 17-25) which is asserted when a branch is determined to have been mispredicted, and deasserted when the prediction is correct. Parady in view of Bondi, as shown above, has taught the detection of mispredicted branch events in order to minimize the performance penalty suffered by a misprediction. One of ordinary skill in the art would have recognized that the only way to detect a mispredicted branch is to execute the conditional branch instruction to get the result and compare it against the prediction. Therefore, one of ordinary skill in the art would have found it obvious to modify Parady to include the misprediction signal of Bondi in order to correctly detect a mispredicted branch.

16. Regarding claim 4, Parady in view of Bondi has taught a multi-threading processor as recited in claim 3, wherein the switch logic module includes an outstanding switch request indicator that is set when the switching event does not require an immediate switch (see Parady, Col.1 lines 45-57 and Col.4 lines 53-62). For the case of a non-blocking load, there does not need to be an immediate switch. While not taught explicitly, there inherently must be a signal that is set to distinguish between blocking and non-blocking loads so that the processor knows if it can continue executing. This can be considered an outstanding switch request indicator

because if it is a blocking load, this signal will be deasserted and not affect the normal thread switching operations.

17. Regarding claim 6, Parady in view of Bondi has taught a multi-threading processor as recited in claim 1, wherein the state module includes a pair of register files (48 and 50 of Fig.3) and a pair of IPs (110 of Fig.3).

18. Regarding claim 7, Parady in view of Bondi has taught a multi-threading processor as recited in claim 6, wherein the IPs are coupled to the front-end module and the register files are coupled to the execution module (see Fig.3).

19. Regarding claims 9 and 15, taking claim 9 as exemplary, Parady in view of Bondi has taught a method for concealing switch latency in a multi-threading processor as recited in claim 8, further comprising executing a switch to another software thread if the switching event requires an immediate switch (see Parady, Col.1 lines 45-57 and Col.4 lines 53-62).

20. Claim 15 is nearly identical to claim 9. It differs only in its parent claim, but encompasses the same scope. Therefore, claim 15 is rejected for the same reasons as claim 9.

21. Claims 5, 10-13 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627, in further view of Bondi et al., U.S. Patent No. 5,881,277 as applied to claims 1-3 above, and further in view of Borkenhagen et al., U.S. Patent No. 6,567,839.

22. Regarding claims 5, 10 and 16, taking claim 5 as exemplary, Parady in view of Bondi has taught a multi-threading processor as recited in claim 4, but has not taught wherein the switch logic module includes a counter to schedule a switch based on a time quantum.

23. However, Borkenhagen has taught the scheduled switching between threads based on a time quantum and a countdown register to prevent threads from being inactive too long while processing a long-latency event (see Col.5 lines 50-57, Col.6 lines 32-35, and Col.18 lines 15-21). One of ordinary skill in the art would have recognized that inactive or stalled threads are wasting valuable processor cycles that could be spent processing other data. Therefore, one of ordinary skill in the art would have found it obvious to modify the multi-threaded processor as taught by Parady in view of Bondi to include the scheduled thread switching based on the a time quantum of Borkenhagen in order to force inactive threads to switch to new active threads, thus improving processor throughput and reducing wasted processor cycles.

24. Claims 10 and 16 are nearly identical to claim 5. While they differ in their parent claims, both claims encompass the scope of claim 5. Therefore, claims 10 and 16 are rejected for the same reasons as claim 5.

25. Regarding claims 11 and 17, taking claim 11 as exemplary, Parady in view of Bondi, in further view of Borkenhagen has taught a method for concealing switch latency in a multi-threading processor as recited in claim 10, wherein the switch takes place "rapidly" (see Borkenhagen, Col.4 lines 38-41). Parady in view of Bondi in further view of Borkenhagen has not explicitly taught wherein the switch has a latency of about 15 to about 20 clocks.

26. However, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to make a switch with a latency of about 15 to about 20 clocks because the Applicant has not disclosed that doing so provides an advantage, is used for a particular purpose, or solves a stated problem. Furthermore, one of ordinary skill in the art would have expected Applicant's invention to perform equally well with either the "rapidly" switching

between threads taught by Borkenhagen or the claimed about 15 to about 20 clocks because both latencies perform the same function of providing a thread switch with minimal latency. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady in view of Bondi in further view of Borkenhagen to obtain the invention as specified in claim 11.

27. Claim 17 is nearly identical to claim 11. It differs only in its parent claim, but encompasses the same scope. Therefore, claim 17 is rejected for the same reasons as claim 11.

28. Regarding claims 12 and 18, taking claim 18 as exemplary, Parady in view of Bondi, in further view of Borkenhagen has taught a method for concealing switch latency in a multi-threading processor as recited in claim 11, wherein the time quantum can be customized according to a specific hardware configuration (see Borkenhagen, Col.18 lines 15-21, 36-38). Parady in view of Bondi in further view of Borkenhagen has not explicitly taught wherein the time quantum is less than about 1,000 clocks.

29. However, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to make the time quantum less than about 1,000 clocks because the Applicant has not disclosed that doing so provides an advantage, is used for a particular purpose, or solves a stated problem. Furthermore, one of ordinary skill in the art would have expected Applicant's invention to perform equally well with either a "customized" time quantum or the claimed less than about 1,000 clocks because both quantums perform the same function of providing a time-out value to force a thread switch. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady in view of Bondi in further view of Borkenhagen to obtain the invention as specified in claim 12.

30. Claim 18 is nearly identical to claim 12. It differs only in its parent claim, but encompasses the same scope. Therefore, claim 18 is rejected for the same reasons as claim 12.

31. Regarding claims 13 and 19, taking claim 19 as exemplary, Parady in view of Bondi in further view of Borkenhagen has taught a method for concealing switch latency in a multi-threading processor as recited in claim 12, wherein the time quantum can be customized according to a specific hardware configuration (see Borkenhagen, Col.18 lines 15-21, 36-38). Parady in view of Bondi in further view of Borkenhagen has not explicitly taught wherein the time quantum is about 200 clocks.

32. However, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to make the time quantum is about 200 clocks because the Applicant has not disclosed that doing so provides an advantage, is used for a particular purpose, or solves a stated problem. Furthermore, one of ordinary skill in the art would have expected Applicant's invention to perform equally well with either a "customized" time quantum or the claimed about 200 clocks because both quantums perform the same function of providing a time-out value to force a thread switch. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady in view of Bondi in further view of Borkenhagen to obtain the invention as specified in claim 13.

33. Claim 19 is nearly identical to claim 13. It differs only in its parent claim, but encompasses the same scope. Therefore, claim 19 is rejected for the same reasons as claim 13.

Conclusion

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

35. Joy et al., U.S. Patent No. 6,341,347, has taught thread switching logic that performs fast thread switching in response to a long latency cache miss.

36. Nuechterlein et al., U.S. Patent No. 6,594,755, has taught a thread switch upon the detection of a branch instruction in the instruction flow.

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
11/25/2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100